

What is claimed is:

1. An emitter for an electron-beam projection lithography (EPL) system comprising:
 - 5 a substrate;
 - an insulating layer overlying the substrate; and
 - a gate electrode comprised of a base layer formed on the insulating layer to a uniform thickness and an electron-beam blocking layer formed on the base layer in a predetermined pattern.
- 10 2. The emitter of claim 1, wherein the insulating layer is made of a silicon oxide layer.
- 15 3. The emitter of claim 1, further comprising a lower electrode between the substrate and the insulating layer.
4. The emitter of claim 3, wherein the insulating layer is made from an anodized metal.
- 20 5. The emitter of claim 1, wherein the base layer is made of a conductive metal, and the electron-beam blocking layer is made of a metal capable of anodizing.
- 25 6. The emitter of claim 5, wherein the base layer is made of a metal selected from the group consisting of gold (Au), platinum (Pt), aluminum (Al), titanium (Ti), and tantalum (Ta).
7. The emitter of claim 5, wherein the electron-beam blocking layer is made of a metal selected from the group consisting of titanium (Ti), aluminum (Al),

and ruthenium (Ru).

8. The emitter of claim 3, wherein the base layer is made of a conductive metal, and the electron-beam blocking layer is made of a metal capable of
5 anodizing.

9. The emitter of claim 8, wherein the base layer is made of a metal selected from the group consisting of gold (Au), platinum (Pt), aluminum (Al), titanium (Ti), and tantalum (Ta).

10 10. The emitter of claim 8, wherein the electron-beam blocking layer is made of a metal selected from the group consisting of titanium (Ti), aluminum (Al), and ruthenium (Ru).

15 11. The emitter of claim 1, wherein the base layer and the electron-beam blocking layer of the gate electrode are made of silicon.

12. The emitter of claim 3, wherein the base layer and the electron-beam blocking layer of the gate electrode are made of silicon.

20 13. A method of manufacturing an emitter for an electron-beam projection lithography (EPL) system, the method comprising steps of:

(a) preparing a substrate;

(b) forming an insulating layer on the substrate;

25 (c) forming a base layer of a gate electrode by depositing a conductive metal on the insulating layer to a predetermined thickness;

(d) forming an electron-beam blocking layer of the gate electrode by depositing a metal capable of anodizing on the base layer to a predetermined thickness; and

(e) patterning the electron-beam blocking layer in a predetermined pattern by anodizing.

14. The method of claim 13, wherein the substrate is a silicon wafer.

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15. The method of claim 14, wherein the insulating layer is made of a silicon oxide layer formed by thermally oxidizing the surface of the silicon wafer.

16. The method of claim 13, before step (b), further comprising step of forming a lower electrode on the substrate.

17. The method of claim 16, wherein, in step (b), the insulating layer is formed by depositing a metal capable of anodizing on the lower electrode and anodizing the metal.

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18. The method of claim 13, wherein in step (c), the conductive metal is selected from the group consisting of gold (Au), platinum (Pt), aluminum (Al), titanium (Ti), and tantalum (Ta).

20 19. The method of claim 13, wherein in step (d), the metal capable of anodizing is selected from the group consisting of titanium (Ti), aluminum (Al), and ruthenium (Ru).

25 20. The method of claim 13, wherein step (e) comprises steps of:
anodizing the electron-beam blocking layer in a predetermined pattern by scanning probe microscope (SPM) lithography; and
removing the anodized portion of the electron-beam blocking layer by etching.

21. The method of claim 13, wherein step (e) comprises steps of:

coating a resist on the surface of the electron-beam blocking layer;
patterning the resist in a predetermined pattern;
anodizing a portion of the electron-beam blocking layer exposed by patterning
of the resist; and

5 removing the anodized portion of the electron-beam blocking layer by etching
and cleaning off the resist.

22. A method of manufacturing an emitter for an electron-beam projection
lithography (EPL) system, the method comprising steps of:

10 (a) preparing a substrate;
(b) forming an insulating layer on the substrate;
(c) depositing a first silicon layer on the insulating layer to a uniform
thickness;
(d) patterning the first silicon layer in a predetermined pattern; and
15 (e) depositing a second silicon layer on the insulating layer exposed in step
(d) and first silicon layer and forming a gate electrode comprised of the first and
second silicon layers.

23. The method of claim 22, wherein the substrate is a silicon wafer.

20 24. The method of claim 23, wherein the insulating layer is made of a
silicon oxide layer formed by thermally oxidizing the surface of the silicon wafer.

25 25. The method of claim 22, before step (b), further comprising step of
forming a lower electrode on the substrate.

26. The method of claim 25, wherein, in step (b), the insulating layer is
formed by depositing a metal capable of anodizing on the lower electrode and
anodizing the metal.

27. The method of claim 22, wherein step (d) comprises steps of:
coating a resist on the surface of the first silicon layer;
 patterning the resist in a predetermined pattern; and
 etching the first silicon layer using the resist as an etch mask.